Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-21. Cancelled.

22. (Currently amended) Apparatus for performing start-up AFC during initial cell search (ICS) by a user equipment (UE) receiver, where the ICS comprises:

a ~~Step-1~~ processor ~~for Step-1 processing of~~ configured to process a ~~given~~ received synchronization code sequence to provide a peak location of the received synchronization code sequence;

a first correlator for determining a correlation between ~~said given~~ the received synchronization code sequence and a ~~stored~~ sequence generated by the apparatus;

a second correlator for determining a correlation between ~~said given~~ the synchronization code sequence and ~~the stored~~ a sequence equivalent to the generated sequence which has been altered in phase;

an error estimator for determining the error associated with the outputs of the first and second correlators;

said error estimator including:

estimator ciruitry configured to provide first, second and third offset estimates; and

a combiner configured to combine said first, second and third offset estimates to produce the error estimate;

a filter for selectively integrating the error estimate responsive to an initial or steady state conditions of the cell search process; and

~~one of a voltage controlled~~ an oscillator ~~(VCO) and a numeric controlled oscillator (NCO) for adjusting~~ configured to produce an adjusted frequency responsive to the integrated error estimate~~;~~

~~said error estimator further comprising:~~

~~an estimator for providing first, second and third offset estimates; and~~

~~an averager for averaging said first, second and third offset estimates~~.

23. (Currently amended) The apparatus of claim 22 wherein:

said estimator circuitry is configured to provide as the first, second and third offset estimates respective ~~are~~ early, punctual and late estimates;

said combiner is a summer configured to sume said early, punctual and late estimates to produce the error estimate; and

said oscillator is one of a voltage control oscillator (VCO) and a numeric controlled oscillator (NCO).

24. (Currently amended) The apparatus of claim 23 wherein ~~the~~ said estimator circuitry ~~for providing early, punctual and late estimates~~ comprises:

an early estimator for providing an early estimate which is offset $-\frac{1}{2}T_C$ relative to ~~the~~ a punctual estimate and a late estimator to provide a late estimate which is offset $+\frac{1}{2}T_C$ relative to the punctual estimate wherein T_C is no greater than ½ of a sampling rate.

25.-26. Cancelled.

27. (Currently amended) Apparatus for performing start up automatic frequency control (AFC) during an initial cell search (ICS) by a user equipment (UE) receiver comprising:

a ~~Step 1~~ processor ~~for performing Step 1 processing of~~ configured to process a received code sequence to provide a location of a synchronization channel;

a sequence locator and splitter responsive to a location output of said Step 1 processor ~~for producing~~ configured to produce early, punctual and late frequency offsets based on the received sequence;

first, second and third frequency estimators ~~respectively determining an estimated frequency~~ configured to determine respective early, punctual and late frequency estimates from said early, punctual and late offsets;

a combiner configured to combine the early, punctual and late frequency estimates to produce an error estimate;

~~an averager for averaging the estimated frequencies~~;

a filter for selectively integrating the error estimate; and

~~one of a voltage control~~ an oscillator ~~(VCO) and a numeric controlled oscillator (NCO) for adjusting~~ configured to produce an adjusted frequency of the receiver responsive to the integrated error estimate.

28. (Currently amended) A method of performing start-up automatic frequency control (AFC) for use during initial cell search (ICS) processing by a user equipment (UE) receiver, ~~where the ICS processing comprises Step 1 processing of a received primary synchronization code (PSC) sequence~~, the method comprising:

(a) receiving ~~said~~ a received primary synchronization code (PSC) sequence which has a received frequency, and ~~performing Step 1~~ processing ~~of~~ the received PSC sequence to form a first estimate of the received frequency;

(b) rotating a phase of a stored sequence at the estimated received frequency plus a given frequency amount, to form an increased rotated phase of the stored sequence;

(c) rotating a phase of the stored sequence at the estimated received frequency minus the given frequency amount, to form a decreased rotated phase of the stored sequence;

(d) correlating each of early, punctual and late offsets of the received PSC sequence with the increased rotated phase of the stored sequence, and correlating each of the early, punctual and late offsets of the received PSC sequence with the decreased rotated phase of the stored sequence;

(e) combining ~~the two~~ respective pairs of correlations from step (d) to form early, punctual and late estimates, combining the early, punctual and late estimates, and producing a frequency adjustment value from the combined early, punctual and late estimates, and

(f) revising the estimated received frequency and adjusting the UE receiver, responsive to the frequency adjustment value.

29. (Previously presented) The method of claim 28, further comprising repeating steps (b) through (f) a preferred number of times.

30. (Previously presented) The method of claim 29, wherein the preferred number of times is 24.

31. (Currently amended) A user equipment (UE) for performing start-up automatic frequency control (AFC) during initial cell search (ICS) processing ~~according to the method of claim 28, where the ICS processing comprises Step 1 processing of a received primary synchronization code (PSC) sequence~~, the UE comprising:

~~(a)~~ a receiver ~~for receiving said~~ configured to receive a received primary synchronization code (PSC) sequence which has a received frequency;

~~(b)~~ a ~~Step 1~~ processor ~~for performing Step 1 processing of~~ configured to process the received PSC sequence to form a first estimate of the received frequency;

~~(c) a storage device for storing a sequence;~~

~~(d) an increased phase rotator for rotating a phase of the stored sequence at the estimated received frequency plus a given frequency amount, to form an increased rotated phase of the stored sequence;~~

~~(e) a decreased phase rotator for rotating a phase of the stored sequence at the estimated received frequency minus the given frequency amount, to form a decreased rotated phase of the stored sequence;~~

~~(f) a first correlator for correlating the received PSC sequence with the increased rotated phase of the stored sequence;~~

~~(g) a second correlator for correlating received PSC sequence with the decreased rotated phase of the stored sequence;~~

~~(h) an integrator for combining the two correlations from steps (f) and (g) to form a frequency adjustment value;~~

~~(i)~~ an estimated frequency reviser ~~for revising the estimated received frequency responsive to the~~ configured to produce a frequency adjustment value;

said estimated frequency reviser including:

a first frequency estimator configured to produce an estimate of an early offset of the received PSC sequence;

a second frequency estimator configured to produce an estimate of a punctual offset of the received PSC sequence;

a third frequency estimator configured to produce an estimate of a late offset of the received PSC sequence; and

a combiner configured to combine the estimates produced by said first second and third frequency estimators to produce a combined error estimate from which the frequency adjustment value is produced; and

~~(j)~~ a receiver adjuster ~~for adjusting~~ configured to the UE receiver, responsive to the frequency adjustment value.

32. (Currently amended) The UE of claim 31, wherein:

at least on of said frequency estimator includes:

a storage device for storing a sequence;

an increased phase rotator configured to rotate a phase of the stored sequence at the estimated received frequency plus a given frequency amount, to form an increased rotated phase of the stored sequence;

a decreased phase rotator configured to rotate a phase of the stored sequence at the estimated received frequency minus the given frequency amount, to form a decreased rotated phase of the stored sequence;

a first correlator configured to correlate the received PSC sequence with the increased rotated phase of the stored sequence;

a second correlator configured to correlate the received PSC sequence with the decreased rotated phase of the stored sequence; and

an integrator configured to combine correlations from said first and second correlators;

said combiner is configured as a summer; and

the receiver adjuster ~~of step (j)~~ is one of a voltage controlled oscillator (VCO) and a numerical controlled oscillator (NCO).

33. (Currently amended) The UE of claim 31, further comprising ~~a~~ repeater circuitry configured to repetitively operate said estimated frequency reviser during ISC processing ~~for repeating steps (b) through (f)~~.

34. (Currently amended) ~~The UE of claim 33, further comprising~~

A user equipment (UE) for performing start-up automatic frequency control (AFC) during initial cell search (ICS) processing comprising:

a receiver configured to receive a received primary synchronization code (PSC) sequence which has a received frequency;

a processor configured to process the received PSC sequence to form a first estimate of the received frequency;

a storage device configured to store a sequence;

an increased phase rotator configured to rotate a phase of the stored sequence at the estimated received frequency plus a given frequency amount, to form an increased rotated phase of the stored sequence;

a decreased phase rotator configured to rotate a phase of the stored sequence at the estimated received frequency minus the given frequency amount, to form a decreased rotated phase of the stored sequence;

a first correlator configured to correlate the received PSC sequence with the increased rotated phase of the stored sequence;

a second correlator configured to correlate received PSC sequence with the decreased rotated phase of the stored sequence;

an integrator configured to combine the correlations from said first and second correlators to form a frequency adjustment value;

an estimated frequency reviser configured to revise the estimated received frequency responsive to the a frequency adjustment value;

a receiver adjuster configured to the UE receiver, responsive to the frequency adjustment value;

repeater circuitry configured to repetitively operate said phase rotators, correlators, integrator and estimated frequency reviser during ISC processing; and

a counter associated with said repeater circuitry to repetitively operate said phase rotators, correlators, integrator and estimated frequency reviser during ISC processing ~~whereby steps (b) through (f) are repeated~~ a preferred number of times.

35. (New) The UE of claim 33, further comprising a counter associated with said repeater circuitry to repetitively operate said estimated frequency reviser during ISC processing ~~whereby steps (b) through (f) are repeated~~ a preferred number of times.